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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,928	03/31/2001	John T. Orchard	15685P096	7550

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EXAMINER	
NGO, CHUONG D	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 09/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,928	ORCHARD, JOHN T.	
	Examiner	Art Unit	
	Chuong D Ngo	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,4-17 and 19-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,4-17 and 19-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 2,4-17, and 19-31 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Grisamore (6,535,901).

As per claims 2,11,12,14-17,26,27 and 29-31, Grisamore discloses in figures 5 and 9 a method for implementing a Wallace-architecture in which full-adders (3-dot circle) and half adders (2-dot circle) are selected and their numbers are clearly depend on a bit-wise analysis of the input terms within each level of bit-significance. It is noted that Grisamore does not teach registers in figures 5 and 9. However, Grisamore discloses that it is known in the art to use registers at optimal points in a multiplier to enable pipelined processing which provides a high through put multiply accumulate circuit. Thus it would have been obvious to a person of ordinary skill in the art to provides the Wallace-architecture of Grisamore with registers at optimal points in the architecture to enable pipelined processing in order increase the through put of circuit.

As per claims 4,13,19-25 and 28, since it is well know in the art to implement a multiplier by a FPGA (see the cited references), It would have been obvious to a person of ordinary skill in the art, as a matter of design choice, to implement the multiplier by a FPGA as claimed.

2. Claims 2,4-17 and 19-31 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Costa et al. (5,935,201).

As per claims 2,11,12,14-17,26,27 and 29-31, Costa et al. discloses in figures 7-9 a Wallace-architecture in which full-adders (3-input block) and half adders (2-input block) are selected and their numbers are clearly depend on a bit-wise analysis of the input terms within each level of bit-significance. It is noted that Costa et al does not teach registers in the Wallace-architecture. However, since it is known in the art to use registers at optimal points in a multiplier to enable pipelined processing which provides a high through put multiply circuit. Thus, it would have been obvious to a person of ordinary skill in the art to provides the Wallace-architecture of Costa et al. with registers at optimal points in the architecture to enable pipelined processing in order increase the through put of circuit.

As per claims 4,13,19-25 and 28, since it is well know in the art to implement a multiplier by a FPGA (see the cited references), It would have been obvious to a person of ordinary skill in the art, as a matter of design choice, to implement the multiplier by a FPGA as claimed.

3. Applicant's arguments filed on 05/25/2004 have been fully considered but they are not persuasive. It is respectfully submitted that both figure 5 of Grisamore and figure 8 of Costa full-adders (FAs) and half adders (HAs3) are selected and their numbers are clearly depend on a bit-wise analysis of the input terms within each level of bit-significance. For instance, in figure 5 of Grisamore the number of full-adders and half adders in each column (level of bit-significance) is not arbitrary, but are differently selected for each column depend on the number of product terms in that column. For example in figure 5 of Grisamore, there is a HA in column 1 having three product terms, a HA and a FA in column 2 having four product

terms, and a HA and two FAs in column 3 having 5 product terms, etc. Changing the number of product terms in a column would clearly change the numbers of FA and HA in that column. The statement in Grisamore that "the process then continues by determining number of, and configuration of, full adders and half adders required for a reduction function of the current partial products based on the one of the plurality of reduction patterns and the size of the current partial products" is a general teaching. It should be noted that the required numbers of full adders an half adders are depend on the numbers of full adders an half adders in each column (level of bit-significance), and the size of the current partial products is depend on the number of product terms in each column. Figure 5 of Grisamore discloses in details the circuit design in which full-adders (FAs) and half adders (HAs) are selected and their numbers for each column (level of bit-significance) are clearly depend on the number of product terms in that column, and that clearly requires a bit-wise analysis of the input terms within each level of bit-significance (column) as claimed.

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

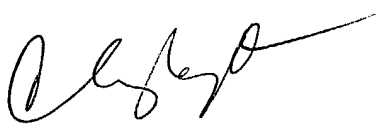
however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong D Ngo whose telephone number is (703) 305-9764. The examiner can normally be reached on Tuesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703) 309-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Chuong D Ngo
Primary Examiner
Art Unit 2124

02/20/2004